IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A method for analyzing circuit designs, comprising the steps of:

discretizing a design representation into pixel elements representative of a structure in the design where each pixel element represents a portion of the design;

determining at least one property for each pixel element representing the portion of the design where the at least one property is represented by an intensity of the pixel element, such that the pixel elements provide a pixel map to visually represent the design representation based on the at least one property; and

determining a response of the design due to local properties across the design based upon representations of the pixel elements.

2. (Original) The method as recited in claim 1, further comprising the step of exporting pixel properties to an application.

3. (Original) The method as recited in claim 1, further comprising the step of assembling pixel properties to determine local three-dimensional properties.

4. (Original) The method as recited in claim 3, wherein the step of determining a response of the design due to local properties across the design includes the step of determining a global response for an architecture due to the local three-dimensional properties.

5. (Original) The method as recited in claim 1, further comprising the step of importing a design to be analyzed.

6. (Original) The method as recited in claim 5, wherein the design includes a computer generated design of one of a circuit and a chip.

7. (Original) The method as recited in claim 1, wherein the at least one property includes metal fraction and the global response includes thermal strain.

8. (Original) The method as recited in claim 1, wherein the step of determining a response of the design includes accepting or rejecting a design based on the response.

9. (Original) The method as recited in claim 8, further comprising the step of altering a design based on the response.

10. (Original) The method as recited in claim 1, wherein the step of determining a response further includes representing a three-dimensional multi-layered design in two dimensions such that properties within all layers are accumulated and represented in the two-dimensional image.

11. (Previously Presented) A program storage device readable by machine, tangibly

embodying a program of instructions which when executed by the machine ~~to~~ performs method steps for analyzing circuit designs, as recited in claim 1.

12. (Previously Presented) The method as recited in claim 1, wherein the at least one property includes metal fraction information relating to the metal fraction of stacked via structures.

13. (Previously Presented) A method for analyzing circuit designs, comprising the steps of:

discretizing a design representation into pixel elements representative of a structure in the design where each pixel element represents a portion of the design;

analyzing properties in each pixel element to represent the properties by an intensity of the pixel element, such that the pixel elements provide a pixel map to visually represent the design representation based on the properties;;

assembling pixel properties to determine properties of a local three-dimensional circuit architecture; and

determining a global response of the circuit architecture due to local properties across the design based upon representations of the pixel elements.

14. (Original) The method as recited in claim 13, further comprising the step of exporting pixel properties to an application.

15. (Original) The method as recited in claim 13, further comprising the step of importing

a design to be analyzed.

16. (Original) The method as recited in claim 15, wherein the design includes a computer generated design of one of a circuit and a chip.

17. (Previously Presented) The method as recited in claim 13, wherein the properties include metal fraction and the global response includes thermal strain.

18. (Original) The method as recited in claim 13, wherein the step of determining a global response of the design includes accepting or rejecting a design based on the global response.

19. (Original) The method as recited in claim 18, further comprising the step of altering a design based on the global response.

20. (Original) The method as recited in claim 13, wherein the step of determining a response further includes representing a three-dimensional multi-layered design in two dimensions such that properties within all layers are accumulated and represented in the two-dimensional image.

21. (Previously Presented) A program storage device readable by machine, tangibly embodying a program of which when executed by the machine performs method steps for analyzing circuit designs, as recited in claim 13.

22. (Previously Presented) The method as recited in claim 13, wherein the properties in each pixel element include metal fraction information relating to the metal fraction of stacked via structures.

23. (Currently Amended) A method for analyzing circuit designs, comprising the steps of:

importing a digitally rendered representation of a design;

discretizing the design representation into pixel elements representative of a structure in the design where each pixel element represents a portion of the design;

analyzing properties in each pixel element by calculating the properties based on geometrical features in the design where the properties are represented by an intensity of the pixel element, such that the pixel elements provide a pixel map to visually represent the design representation based on the at least one property;

assembling pixel properties in geometrical regions to determine properties of a local three-dimensional circuit architecture; and

determining a global response of the circuit architecture due to the local properties across the design based upon representations of the pixel elements.

24. (Original) The method as recited in claim 23, further comprising the step of exporting pixel properties to an application.

25. (Original) The method as recited in claim 23, wherein the design includes the design of a circuit or a chip.

26. (Previously Presented) The method as recited in claim 23, wherein the properties include metal fraction and the global response includes thermal strain.

27. (Original) The method as recited in claim 23, wherein the step of determining a global response of the design includes accepting or rejecting a design based on the global response.

28. (Original) The method as recited in claim 23, further comprising the step of altering a design based on the global response.

29. (Original) The method as recited in claim 23, wherein the step of determining a response further includes representing a three-dimensional multi-layered design in two dimensions such that properties within all layers are accumulated and represented in the two-dimensional image.

30. (Previously Presented) A program storage device readable by machine, tangibly embodying a program of instructions which when executed by the machine ~~to~~ performs method steps for analyzing circuit designs, as recited in claim 23.

31. (Previously Presented) The method as recited in claim 23, wherein the properties include metal fraction information relating to metal fraction generated for the location and number of stacked

via structures.

32. (Currently Amended)) A method for analyzing circuit designs, comprising the steps of:

discretizing a design representation into pixel elements representative of a structure in the design where each pixel element represents a portion of the design;

determining at least one property for each pixel element representing a portion of the design wherein the at least one property includes metal fraction information relating to a metal fraction of structures in the portion, such that the pixel elements provide a pixel map to visually represent the design representation based on the metal fraction information; and

determining a response of the design due to local properties across the design.